What is claimed is

1. A time measurement circuit comprising:

a) a clock input;

b) a delay chain having an input connected to the clock input, the delay chain having a plurality of delay elements each having an output and a tap at the output of each delay element;

c) a STOP input;

d) a second plurality of delay elements, each having an input and an output and each providing a delay between the input and output, wherein the input of each of the second plurality of delay elements is coupled to the STOP input; and

e) a coincidence circuit having a first plurality of inputs, each coupled to one of the taps and a second plurality of inputs, each coupled to the output of one the second plurality of delay elements, and an output, the output representing the coincidence between one of the taps and one of the outputs of the second plurality of delay elements.

2. The time measurement circuit of claim 1 wherein the coincidence circuit comprises a plurality of column circuits, each having an input connected to one of the taps and a second set of inputs, each connected to one of the outputs of the second plurality of delay elements.

3. The time measurement circuit of claim 2 wherein each of the column circuit comprises a plurality of logic circuits, each having a first input connected to said tap and a second input, connected one of the outputs of the second plurality of delay elements, and an output reflecting coincidence of the inputs.

4. The time measurement circuit of claim 3 wherein each of the column circuits additionally comprises an encoder circuit, the encoder circuit having a plurality of inputs, each connected to the output of a logic circuit and an output, reflecting coincidence of each of the

5. The time measurement circuit of claim 2 wherein each of the coincidence circuits comprises an encoder and the output of each column circuit has fewer bits than the number of inputs in the second set of inputs.

6. The time measurement circuit of claim 1 wherein the coincidence circuit comprises circuitry producing a first plurality of sets of intermediate signals, each set of intermediate signals representing the coincidence between one of the first plurality of inputs and each of the second plurality of inputs.

7. The time measurement circuit of claim 6 wherein the coincidence circuit additionally comprises an encoder circuit having inputs connected to the sets of intermediate signals and an output reflecting the nominal measured time value.

8. The time measurement circuit of claim 7 additionally comprising a calibration memory, having an input reflecting the nominal time measurement coupled to the encoder circuit and an output reflecting the calibrated time.

9. The time measurement circuit of claim 1 additionally comprising a counter having a count input coupled to said counter and an input for disabling counting coupled to the STOP input.

10. The time measurement circuit of claim 1 wherein each of the elements in the delay chain has a nominal delay of D and the difference between the longest delay and the shortest delay introduced by the second plurality of delay elements exceeds D.

11. The time measurement circuit of claim 1 wherein the delay chain is part of a delay locked loop.

12. A time measurement circuit, comprising:

a) a clock input;

b) a first circuit having an input coupled to the clock and a first plurality of outputs, each representing the clock delayed by a different amount;

c) a STOP input;

d) a second circuit having an input coupled to the STOP input and a second plurality of outputs, each representing the STOP input delayed by a different amount;

e) a third circuit accepting as inputs the outputs of the first circuit and the second circuit, the third circuit having a digital output containing a

plurality of bits that represent coincidence between one of the first plurality of signals and one of the second plurality of signals.

13. The time measurement circuit of claim 12 wherein the first circuit comprises a delay locked loop.

14. The measurement circuit of claim 12 wherein the third circuit comprises a plurality of encoders, each encoding the pattern of bits formed by computing the logical AND between one of the first plurality of outputs and each of the second plurality of outputs.

15. The time measurement circuit of claim 12 wherein the third circuit additionally comprises a calibration memory.

16. The time measurement circuit of claim 12 wherein the time measurement circuit is implemented as a CMOS integrated circuit chip.

17. The time measurement circuit of claim 16, wherein the CMOS integrated circuit is adapted for use in automatic test equipment having a plurality of channel circuits and the integrated circuit chip additionally comprises at least one of the channel circuits.

18. The time measurement circuit of claim 12 used within automatic test equipment, wherein:

a) the test equipment additionally comprises a second time measurement circuit as in claim 12;

b) the time measurement circuit and the second time measurement circuit are connected to a common clock; and

c) the STOP input of the time measurement circuit is connected to a signal that indicates that start of an interval to be measured and the STOP input of the second time measurement circuit is connected to signal that indicates the end of an interval to be measured; and

d) the test equipment additionally comprises a controller, connected to the time measurement circuit and the second time measurement circuit that outputs a time value reflecting the difference in time measured by the second time measurement circuit and the first time measurement circuit.

19. The time measurement circuit of claim 18 wherein the time measurement circuit and the second time measurement circuits each includes a counter connected to the common clock signal.

20. The time measurement circuit of claim 19 wherein the time measurement circuit and the second time measurement circuit and said counters are implemented on a CMOS chip.